WHAT IS CLAIMED IS:

1. A method for forming an alignment pattern of a semiconductor device, the method comprising the steps of:

i) forming a trench in each of a cell area, a peripheral circuit area, and a scribe line of a silicon substrate;

ii) depositing an oxide layer on an entire surface of the silicon substrate in such a manner that the trench formed in the cell area of the silicon substrate is filled with the oxide layer;

iii) forming a trench-type isolation layer in both cell area and peripheral circuit area of the silicon substrate by CMP the oxide layer;

iv) forming an ion implantation mask for exposing predetermined portions of the cell area, the peripheral circuit area formed on the silicon substrate and a trench portion of the scribe line filled with the oxide layer;

v) implanting impurities into an exposed portion of the silicon substrate, which is not covered with the ion implantation mask;

vi) performing the wet dipping for an oxide layer to a resultant structure of the silicon substrate so as to recess the oxide layer filled in the trench of the scribe line; and

vii) removing the ion implantation mask.

2. The method as claimed in claim 1, wherein the ion implantation mask includes a well-forming ion implantation mask or a channel-forming ion implantation mask.

3. The method as claimed in claim 1, wherein the wet dipping for oxide layer is performed in such a manner that a dip out target has thickness no greater than 300Å.

4. The method as claimed in claim 1, wherein the wet dipping for oxide layer is performed by dipping in a solution of NH4F + HF (20:1) for 5~10 seconds.